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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,525	10/08/2003	Varadarajan Srinivasan	NLMI.P133	9642

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EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	10/681,525	SRINIVASAN ET AL.	
	Examiner	Art Unit	
	Gene N. Auduong	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-51 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-51 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/2003 & 01/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on October 8, 2003, October 28, 2003 and January 20, 2004 is being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-17, 24-51 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohira (U.S. Pat. No. 5,602,770).

Regarding claim 1, Ohira discloses a content addressable memory (CAM) device comprising: a first plurality of CAM cells each including a first static storage circuit to store a first data value (figure 1, CAM cells 12; col. 1, lines 11-12, lines 35+); a first pair of bit lines coupled to the first plurality of CAM cells (figure 1, pair of data line DL and its complementary data line /DL); and a first sense amplifier (figure 1, sense amplifier 18 or figure 4a, sense amplifier 18a) including a first transistor 88 having first and second terminals coupled to first and second bit lines, respectively, of the first pair of bit lines (figure 4a, sense amplifier 18a including a first transistor 88 having first and second terminals coupled to first and second data lines DL. /DL of the first data lines pair).

Regarding claim 2, Ohira discloses the CAM device of claim 1 wherein the first sense amplifier 18a further includes a second transistor 84 having first and second terminals coupled to the first and second bit lines, respectively (figure 4a, transistor 84 having first and second terminals coupled to the first and second data lines DL, /DL).

Regarding claim 3, Ohira discloses the CAM device of claim 2 where in the first sense amplifier 18a further includes a third transistor 92 having a first terminal and wherein the first and second transistors 88, 84 have respective third terminals coupled to one another and to the first terminal of the third transistor 92 (figure 4a).

Regarding claim 4, Ohira discloses the CAM device of claim 3 wherein the third transistor 92 has a second terminal coupled to receive a control signal SEN and a third terminal coupled to a reference voltage node (ground potential), the third transistor 92 being switched to a conducting state in response to the control signal SEN to enable the first and second transistors 88, 84 to affect states of the first and second bit lines DL, /DL (figure 4a).

Regarding claim 5, Ohira disclose the CAM device of claim 1 wherein the first terminal of the first transistor 88 is a control terminal, and the second terminal of the second transistor 84 is a control terminal (figure 4a).

Regarding claim 6, Ohira discloses the CAM device of claim 5 wherein the second terminal of the first transistor 88 is an output terminal, and the first terminal of the second transistor 84 is an output terminal (figure 4a).

Regarding claim 7, Ohira discloses the CAM device of claim 1 wherein the first terminal of the first transistor 88 is a gate terminal and the second terminal of the first transistor 88 is a drain terminal (figure 4a).

Regarding claim 8, Ohira discloses the CAM device of claim 7 wherein the first sense amplifier 18a further includes a second transistor 84 having a gate terminal coupled to the second bit line (complementary data line /DL) and a drain terminal coupled to the first bit line (data line DL).

Regarding claim 9, Ohira discloses the CAM device of claim 1 wherein the first static storage circuit (figure 11, storage unit 152) comprises first and second inverters 154a, 154b having respective input and output nodes, the output node of the first inverter 154a being coupled to the input node of the second inverter 154b and the output node of the second inverter 154b being coupled to the input node of the first inverter 154a (figure 11).

Regarding claim 10, Ohira discloses the CAM device of claim 1 wherein the first pair of bit lines DL, /DL is coupled to the first static storage circuit 152 within each of the first plurality of CAM cells (CAM cell 150 of figure 11 or CAM cell 12 of figure 1).

Regarding claim 11, Ohira discloses the CAM device of claim 10 wherein the first static storage circuit (figure 11, storage unit 152) comprises first and second access-enable transistors 156a, 156b, the first access-enable transistor 156a being coupled between the input node of the first inverter 154a and a first bit line (data line DL) of the first pair of bit lines, and the second access-enable transistor 156b being coupled between the input node of the second inverter 154b and a second bit line (complementary data line /DL) of the first pair of bit lines (figure 11).

Regarding claim 12, The CAM device of claim 11 further comprising a first word line WL coupled to control terminal of the first and second access-enable transistors 156a, 156b (figure 11).

Regarding claim 13, Ohira discloses the CAM device of claim 1 further comprising a pair of compare lines coupled to the first plurality of CAM cells 12 or 150, and wherein each of the first plurality of CAM cells 12 or 150 includes a compare circuit coupled to the pair of compare lines and to the first static storage circuit (figure 11, compare circuit (data retrieval unit 154) having a pair of compare lines, (DL, /DL lines also as compare lines for the comparator circuit), connecting to the static storage unit 152).

Regarding claims 14-17, Ohira discloses the CAM device of claim 13 wherein each of the first plurality of CAM cells 12 or 150 further includes a second static storage circuit coupled to the compare circuit of the CAM cell and configured to store a second data value; wherein the second data value is a mask value and wherein the compare circuit includes at least one mask transistor coupled to receive the mask value from the second static storage circuit; a plurality of match lines ML and wherein the compare circuit of each CAM cell 12 or 150 includes first and second transistors coupled in series (figure 11, transistors 158a, 160a coupled in series) between a reference voltage node (figure 11, coupled to ground potential node via transistor 166) and a respective one of the plurality of match lines ML, and third and fourth transistors (figure 11, transistors 158b, 160b) coupled in series between the reference voltage node and a respective one of the plurality of match lines ML, wherein a control terminal of the first transistor 158a is coupled to the first static storage circuit and a control terminal of the third transistor is coupled to the second static storage circuit; and wherein the second transistor 160a is coupled to a first compare line of the pair of compare lines and the fourth transistor 160b is coupled to a second compare line of the pair of compare lines (figure 11; col. 1, lines 35+; col. 8, lines 12+).

Regarding claim 24-26, The CAM device of claim 1 wherein the first sense amplifier (figure 4b, sense amplifier 18b) further includes second and third transistors (transistors 112, 114), the first terminal of the first transistor 110 being coupled to the first bit line DL via the second transistor 112, and the second terminal of the first transistor 110 being coupled to the second bit line /DL via the third transistor 114; wherein the first sense amplifier 18b further includes a fourth transistor 106 having a first and second terminals, the first terminal of the fourth transistor 106 being coupled to the second bit line /DL via the third transistor 114, and the second terminal of the fourth transistor 106 being coupled to the first bit line DL via the second transistor 112; and wherein the first and fourth transistors 110, 106 have respective third terminals coupled to one another (figure 18b).

Claims 27-34, 48-50 and 51 contain the similar limitation as previously discussed in claims 1-17 and 24-26. Therefore, they are analyzed as previously discussed with respect to claims 1-17 and 24-26.

Regarding claims 43-47, the apparatus as previously discussed in claims 1-17, 24-26 and 48-51 would be performed the method as claimed. Therefore, they are analyzed as previously discussed with respect to apparatus claims 1-17, 24-26 and 48-51.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohira (U.S. Pat. No. 5,602,770) in view of Kongetire (U.S. Pat. No. 5,936,873).

Regarding claim 18, Ohira discloses the CAM device having all of the limitation as of claim 1, the CAM cell having its structure conventionally known and used, having the pair compare lines as part of the bitlines pairs and further discloses that the structure of the disclosed CAM cell structure can be replace with other type cell structures or cell type but fails to disclose the CAM cell structure as claimed having a second pair of bit lines; a first transistor coupled between a first bit line of the first pair of bit lines and a first bit line of the second pair of bit lines; and a second transistor coupled between a second bit line of the first pair of bit lines and a second bit line of the second pair of bit lines.

Kongetire discloses a CAM device having the CAM cell structure as claimed in figure 4 having second pair of bitlines 296, 298; a first transistor 320 coupled between a first bit line 230 of the first pair of bit lines and a first bit line 296 of the second pair of bit lines; and a second transistor 322 coupled between a second bit line 232 of the first pair of bit lines and a second bit line 298 of the second pair of bit lines. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ohira's device to substitute the CAM cell having its structure as conventionally known and used, showing in Kongetira's device to have the CAM device with latching sense amplifier as claimed in the CAM cell structure as teaching in Kongetira's device.

Regarding claims 19-21, Ohira in view of Kongetira disclose the CAM device of claim 18 further comprising: a second plurality of CAM cells; a third pair of bit lines coupled to the second plurality of CAM cells; a third transistor coupled between a first bit line of the third pair

of bit lines and the first bit line of the second pair of bit lines; and a fourth transistor coupled between a second bit line of the third pair of bit lines and the second bit line of the second pair of bit lines; wherein the CAM device further comprises a second sense amplifier coupled to the third pair of bit lines; and wherein the second sense amplifier comprises a first transistor having first and second terminals coupled to the first and second bit lines, respectively, of the third pair of bit lines.

Regarding claims 22-23, Ohira in view of Kongetira disclose the CAM device of claim 18 further comprising a second sense amplifier coupled to the second pair of bit lines; wherein the second sense amplifier comprises a first transistor having first and second terminals coupled to the first and second bit lines, respectively, of the second pair of bit lines.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
April 19, 2005

Gene N Auduong
Primary Examiner
Art Unit 2827